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Final Report for Grant ONR N00014-90-J-1114
"Pulse Coded Biologically Motivated Neural-Type MOS Circuits"
For the Period 11/01/89 - 03/31/92

1. Introduction and Main Results

This project has had two aspects, one for ONR and one for AFOSR. The ONR portion was devoted to obtaining hardware implementations for the physiological representations used in the program SYNETSIM developed by the neurophysiologist Dr. D. Hartline of Bekesy Laboratories. The AFOSR portion was for evaluation of the capabilities of pulse coded neural networks.

The main results of this research are:

1. VLSI designs of SYNETSIM modules and their extensions

VLSI Designs for the major pools of SYNETSIM were made and MOSIS fabrications carried out. From these some new elements were designed and in most cases fabricated via MOSIS, the key ones being a neural type arithmetic unit, an adjustable MOSFET transistor convenient for weight setting, and considerable improvement in the neural type cell being used in many of our pulse coded networks. Because capacitors take a large amount of the VLSI chip area, a new capacitance multiplier was designed and fabricated. Using the pools a realization fo ART1 memories was obtained. Means for realizing long term potentiation were investigated which are leading to a new concept of memory based upon the pools and their incorporation of second messenger effects.

2. Pulse coded realizations

A pulse coded neuron for Boolean functions was created and it was shown that any Boolean function of two variables can be computed using it. This leads to the main result that any digital system can be realized as a pulse coded neural network. Similarly a technique for realizing any neural network in pulse coded form has been developed with investigations for a formal proof initiated.

3. Improvements in SYNETSIM and cross fertilizations between neurophysiology and electrical engineering

Primarily the electrical engineering researchers have made many improvements in the user interface of SYNETSIM so that other than neurophysiologists can be comfortable in using SYNETSIM. Among these improvements are the introduction of a netlist format to translate neural network structure into the numerical data used by SYNETSIM, improved input and readout, and incorporation of modulation of all parameters via introduction of a modular form to the program.

4. Incorporation in Neural Type Microsystems

Some of the modules of SYNETSIM are not directly convenient for realization in VLSI form. But by taking the ideas behind the modules and reformulating them into our Neural-Type Microsystems framework we are able to incorporate the desired behavior in simple circuits. For example this has led to new neural type cells, the primary components of our neural systems. And very significantly it has led to investigation of means to realize long term potentiation and memory in neural type microsystems.

In undertaking these results a large number of individuals were involved with eleven University of Maryland researchers financially supported at various points in the research including some very motivated undergraduates. Several researchers at other institutions have entered cooperatively into these research activities leading to a number of cross fertilizations; among these are Dr. D. Hartline and his researchers of the Bekesy Laboratories of the University of Hawaii and Professor M. Zaghloul and her students at George Washington University. One Ph.D. and one MS degree were awarded based upon this research with a number of seminar presentations given as well as papers presented at international meetings and in internationally recognized journals (see listing below). The research has led to a number of new research areas which are planned for future study, including that of modeling live neurons on a chip and new concepts of memory adjustment.

Funded participating researchers with their concentration areas:

I. Primary researchers
   a. Prof. R. Newcomb, PI
      Oversight, circuit and SYNETSIM realizations
   b. Ms. N. El-Leithy, Co-PI
      Long Term Potentiation research
   c. Mr. S. W. Tsay, RA - ONR portion
      VLSI circuit realizations - Ph.D. obtained
   d. Mr. M. de Savigny, RA - AFOSR portion
      Pulse coding vs voltage levels - MS obtained

II. Supplementary researchers
   e. Ms. Shilpa Mehta - undergraduate Honor's Fellow
      DRIVER circuit and neurons on a chip simulations
   f. Ms. Shapna S. Pal - undergraduate researcher
      DRIVER circuit and neurons on a chip simulations
   g. Mr. Jen-dong Yuh, RA (Ph.D. Candidate)
      VLSI and multilevel neurons
   h. Dr. George Syrmos - postdoctoral
      Applications of pulse coded neural networks to robotics
   i. Mr. Samer Minkara, RA (Ph.D. Candidate)
      Soliton realizations for pulse coding
   j. Ms. Louiza Sellami, RA (Ph.D. Candidate)
      Hair cell neural interfacing
   k. Mr. Gregory Wolodkin, RA (MS Candidate, summer at Bekesy)
      User friendly improvements of SYNETSIM

In addition a number of other graduate and undergraduate students indirectly participated through research seminars and design course activities with significant contributions made by P. Bey, S. Lin and L. Chen. Some of these students continue to participate through independent study projects on related topics which have resulted from the research. A number of technical meetings were attended including one involving a large number of internationally known cell neurophysiologists associated with the "Decade of the Brain" celebrations.

2. Theses

The following two theses, which were finished in April 1991, are based upon research under this Grant.

a) S.-W. Tsay, "Design of Neural Chemical Pools for VLSI and Their Applications," Doctoral Dissertation, University of Maryland, May 1991 graduation.

b) M. de Savigny, "Pulse Coded Neuron Realizing Digital Functions," MS Thesis, University of Maryland, May 1991 graduation.

3. Publications

A. Appearing

a) S.-W. Tsay, N. El-Leithy, and R. W. Newcomb, "CMOS Realization of a Class of Hartline Neural Pools," Proceedings of the 1990 IEEE International Symposium on Circuits and Systems, New Orleans, May 1990, pp. 2417 - 2420.

b) G. Wolodkin, N. El-Leithy, M. de Savigny, S. W. Tsay, and R. Newcomb, "A Semistate Description for Hysteresis in MOS Neural-Type Cells," Proceedings of the 33rd Midwest Symposium on Circuits and Systems, Calgary, August 1990, pp. 289 - 292.

c) M. de Savigny, G. Moon, N. El-Leithy, M. Zaghloul, and R. W. Newcomb, "Hysteresis Turn-On-Off Voltages for a Neural-Type Cell," Proceedings of the 33rd Midwest Symposium on Circuits and Systems, Calgary, August 1990, pp. 37 - 39.

d) S. W. Tsay and R. Newcomb, "VLSI Implementation of ART1 Memories," IEEE Transactions on Neural Networks, Vol. 2, No. 2, March 1991, pp. 214 - 221.

e) S. W. Tsay, M. de Savigny, N. El-Leithy, and R. Newcomb, "An all MOS Neural-Type Cell," 34th Midwest Symposium on Circuits and Systems, May 1991, to appear.

f) S.-W. Tsay and R. W. Newcomb, "A Neural-Type Pool Arithmetic Unit," Proceedings of the 1991 IEEE International Symposium on Circuits and Systems, Singapore, June 1991, pp. 2518 - 2521.

g) G. Moon, M. Zaghloul, M. de Savigny, and R. W. Newcomb, "Analysis and Operation of a Neural-Type Cell (NTC)," Proceedings of the 1991 IEEE International Symposium on Circuits and Systems, Singapore, June 1991, pp. 2332 - 2334.

h) S. W. Tsay, L. Chen, N. El-Leithy, G. Wolodkin, and R. Newcomb, "Realization of the Driver Neural Network Module," Proceedings of the IV International Symposium on Biomedical Engineering, Penıscola, Spain, September 1991, pp. 480 - 481.

i) Gyu Moon, Mona E. Zaghloul, and Robert W. Newcomb, "VLSI Implementation of Synaptic Weighting and Summing in Pulse Coded Neural-Type Cells," IEEE Transactions on Neural Networks, Vol. 3, No. 3, May 1992, pp. 394 - 403.

j) Suan-Wei Tsay and Robert W. Newcomb, "Implementation of Hartline Pools and Neural-Type Cells by VLSI Circuits," for Advances in Control Networks and Large Scale Parallel Distributed Processing Models edited by Martin D. Fraser

k) Marc de Savigny and Robert W. Newcomb, "Realization of Boolean Functions Using a Pulse Coded Neuron," ISCAS'92, San Diego, May 1992, to appear.

l) Suan-Wei Tsay and Robert W. Newcomb, "An Adjustable Threshold MOSFET," ISCAS'92, San Diego, May 1992, to appear.

m) Jen-dong Yuh and Robert W. Newcomb, "Circuits for Multi-Level Neuron Nonlinearities," IJCNN'92, Baltimore, June 1992, to appear.

B. Drafts in manuscript form

a) M. de Savigny, S. W. Tsay, and R. W. Newcomb, "Capacitance Multipliers for VLSI Integration of Larce C."

b) Marc de Savigny and Robert W. Newcomb, "Realization of Hopfield Networks with Pulse Coded Neurons."

c) Jen-dong Yuh and Robert W. Newcomb, "A Multi-Level Neural Network for A/D Conversion."

Statement A per telecon
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NWW 5/14/92